Technical Reference Note

Rev. 0.0

APPLICATION OVERVIEW:

HPS3KW – I^{2}C Protocol

PRODUCT:

HPS3KW / AA21970

DESCRIPTION:

POWER SUPPLY FIELD REPLACEMENT UNIT (FRU) SIGNALS

Five pins are allocated for the FRU information on the Power Supply connector. One pin is the Serial Clock (SCL). The second pin is used for Serial Data (SDA). Both pins are bi-directional and are used to form a serial I^{2}C bus. Pins 3 through 5 are address lines A0-A2 to indicate to the power supply's EEPROM which position the power supply occupies in the power bay. Power supply shall use 24C03 EEPROM.

A2	A1	A0	Address	A2	A1	A0	Address
Low	Low	Low	0xA0	High	Low	Low	0xA8
Low	Low	High	0xA2	High	Low	High	0xAA
Low	High	Low	0xA4	High	High	Low	0xAC
Low	High	High	0xA6	High	High	High	0xAE[1]

Table 1. FRU Addressing

[1] This is the default EEPROM address if A0, A1, and A2 are left open.

The FRU circuits and Microprocessor circuits inside the power supply must be powered off the 5VSB on the power supply side of the ORing device. The EEPROM Write Protection scheme should be such that it can only be disabled when the power supply is in Test Mode*. A0, A1, and A2 must be pulled High inside the power supply to the EEPROM bias voltage through separate 10KΩ resistors. The SDA and SCL lines must be pulled High inside the power supply through separate 20KΩ resistors. Additionally the end use system shall provide between 5KΩ to 10KΩ pull-up resistors to the 5VSB for the SDA and SCL lines located on the end use system.

* The Write Protection is also disabled when the Power Supply Firmware is doing a self-test. But at this time the I^{2}C bus is not connected to the output connector. See initialization delay.

FRU Data Format - The FRU data format shall be compliant with the IPMI V1.0 specifications.
The current versions of these specifications are available at
http://developer.intel.com/design/servers/ipmi/spec.htm

ASTEC

EMERSON
Network Power

MICROPROCESSOR MONITOR FUNCTIONS

1.1 Initialization Delay

When AC power is initially applied to the power supply, the FRU and the microprocessor reporting functions will not be available to the system I^2C bus for a period of 200mS. During this time the micro controller is loading it's calibration tables from the EERPOM. After this period expires the System has access via the I^2C bus to both devices.

1.2 Microprocessor Reporting Functions

The power supply shall have enhanced monitor and control functions implemented via the I^2C bus. In order to implement the enhanced monitor functionality each supply shall respond to a second set of addresses determined by an offset of 0x30 added to the value of the three addressing lines. The power supply monitor shall operate as an I^2C slave device. Calibration information can be stored in the reserved area of the existing EEPROM but data retrieval must be in such a manner that does not allow more than one master on the bus.

1.3 Power Supply Addresses

A2	A1	A0	ADDRESS
Low	Low	Low	0x30
Low	Low	High	0x32
Low	High	Low	0x34
Low	High	High	0x36
High	Low	Low	0x38
High	Low	High	0x3A
High	High	Low	0x3C
High	High	High	0x3E

Table 2. Power Supply Addressing

1.4 Monitor Functions

Line voltage: The power supply shall report input line voltage from a value of 180Vrms to 265Vrms. The line voltage values shall be reported as a 16-bit word with 1.3v resolution and ±5% of full-scale accuracy of the actual line voltage (13.2V, so limits are 180VAC to 193.2VAC at the low end and 251.8VAC to 265VAC at the high end.).
To achieve the desired accuracy calibration constants may be stored in the EEPROM during final test.

Output current: The power supply shall report output current from a minimum of 10% of maximum surge current to the maximum surge current value. The output current shall be reported in milliAmps with 200mA resolution and ±2% of full-scale accuracy. To achieve the desired accuracy calibration constants may be stored in the EEPROM during final test.

Internal temperatures: The power supply shall report inlet and outlet air temperatures. The temperature span for inlet and outlet temperature should be from $15^{O}C$ to $65^{O}C$ and $25^{O}C$ to $85^{O}C$ respectively with a $1^{O}C$ resolution and ±5% of full-scale accuracy. Additionally, the fan speed control function shall be over-ridden and the fan shall go to full speed if the internal power supply temperatures require it.

1.5 Control Functions

Remote output disable: The supply shall respond to a remote output disable command. On receipt of this command the power supply shall disable it's output. An enable output command shall only be carried out if PSON signal is asserted (low). The actual state of the PSON signal input to the power supply can still be obtained in the power supply status information via I^2C.

Fan Speed Over-ride: This is a second method of forcing the fans to go to full speed. The first method being the power supply internal fan speed control circuitry. The second method is power supply internal temperature over-ride of the fan control signal. The power supply fan speed is a logical "OR" of the two control methods and cannot be forced to operate a lower speed while one of the control methods indicates high-speed operation.

1.6 Communications

The power supply shall be capable of communicating through I^2C bus. The power supplies will respond to their own addresses and to the general call address 0x00. In this way multiple supply power cycling synchronization can take place.

1.6.1 Clock Frequency

The power supply communication through I^2C bus shall be operated on standard mode with SCL Clock Frequency from 10 to 100 kHz.

1.6.2 Power Supply Commands

There are ten commands that the power supply will respond to.

1. SCRC (Set_Control_Register_Command)
2. RSRC (Read_Status_Register_Command)
3. RASDC (Read_Analog_Sensor_Data_Command)
4. TMC (Test_Mode_Command)
5. FDC (Firmware_Debug_Command)
6. FRNC (Firmware_Revision_Number_Command)
7. STMC (System_Test_Mode_Command)
8. STDFC (System_Test_Data_Format_Command)
9. RRAMC (Read_RAM_Command)
10. RSFRC (Read_SFR_Command)

Power supply control commands will be sent as a three byte message whose first two bytes will be same desired command register value followed by the least significant byte of the sum of the first two bytes.

1.6.3 I^2C Communication Interval

The interval between two consecutive I^2C Communications to the power supply shall be at least 50ms to ensure proper monitoring functionality.

1.6.4 I^2C Signal Integrity

The noise on the I^2C bus due to the power supply shall be less than 500 milliVolts peak to peak. This noise measurement shall be made at the power supply output connector using 3.2 K Ohm resistors pulled up to +5v and 20pF ceramic capacitors to power supply Vaux return.

The noise on the Address lines A0, A1, and A2 will be less than 100 milliVolts peak to peak. This noise measurement shall be made at the address lines of the EEPROM Chip and the GND pin of the EEPROM chip.

The noise on the VCC and GND will be less than 100 milliVolts peak to peak. This noise measurement shall be made at the VCC and GND Pins of the Linear Regulator using differential probe.

1.6.5 Power supply Control Status Register

All power supply control and status monitoring is done via this register. Detailed explanation of functions is given below:

BIT 7	*BIT 6*	*BIT 5*	*BIT 4*	*BIT 3*	*BIT 2*	*BIT 1*	*BIT 0*
PSON_STAT	BAD_CAL	FAN_HI	SELFTEST_FAIL	ROUT_DISABLE	OC_TRIP	OV_TRIP	OT_TRIP
R	R	R/W	R	R/W	R	R	R

Control Status Register

- PSON_STAT: This bit is an image of the PSON# signal coming into the power supply from the system.
- BAD_CAL: This bit will be set to indicate a corrupted calibration table. Under this condition the response to a request for analog data shall be all zeros.
- FAN_HI: Setting this bit will cause the fan run full speed. Reading this bit will tell if the fan is running at full speed due to internal temperatures or in response to an I^2C command.
- SELFTEST_FAIL: This bit will be set to indicate a power supply self-test failure. Under this condition the response to a request for analog data shall be all zeros.
- ROUT_DISBLE: Remote Output Disable. Setting this bit will disable the main outputs and clearing this bit will enable the main output.
- OC_TRIP: Over current trip status. This bit is set when the power supply output has been disabled due to an over current event. In this condition, the Inlet Air temperature will be sensed only when the Amber LED is off (Every other second) and the ADC update flag will be set according to the other three ADC channel reading status.
- OV_TRIP: Over voltage trip status. This bit will be set when the power supply outputs have been disabled and the power supply temperature has not reached the trip limits. This is not a direct sensing of the over voltage trip circuit.
- OT_TRIP: Over temperature status. This bit will be set when the power supply outputs have been disabled and the power supply temperature is past the trip limit. This is not a direct sensing of the over temperature trip circuit.

Refer to the next table for the protocol format.

AA21970 Command #1 Set Control Register — **HPS3KW Command #2 Set Control Register**

Start	Slave Address	A	0x01 / 0x02	A	New Control Reg Value	A	New Control Reg Value	A	LSByte of the sum of previous 2 bytes	A	Stop

AA21970 Command #2 Read Control Status Register — **HPS3KW Command #3 Read Control Status Register**

Start	Slave Address	A	0x02 / 0x03	A	Repeated Start	Slave Address + R	A	Status Register	NA	Stop

AA21970 Command #3 - Read Analog Sensor — **HPS3KW Command #1 - Read Analog Sensor**

Start	Slave Address	A	0x03 / 0x01	A	Repeated Start	Slave Address + R	A	First Byte	A	Second Byte	A		Nth Byte	NA	Stop

Command #4 Test Mode

Start	Slave Address	A	0x04	A	0x04	A	0x04	A	LSByte of the sum of previous 2 bytes	A	Stop

Command #5 - Firmware Debug

Start	Slave Address	A	0x05	A	Repeated Start	Slave Address + R	A	First Byte	A	Second Byte	A		8th Byte	NA	Stop

Command #6 - Firmware Revision

Start	Slave Address	A	0x06	A	Repeated Start	Slave Address + R	A	Major Revision	A	Minor Revision	NA	Stop

Command #7 - System Test Mode

Start	Slave Address	A	0x07	A	0x07	A	0x07	A	sum of previous 2 bytes	A	Stop

Command #8 - System Test Data Format

Start	Slave Address	A	0x08	A	FORMAT	A	FORMAT	A	sum of previous 2 bytes	A	Stop

Command #9 - Read RAM

Start	Slave Address	A	0x09	A	OFFSET	A	Repeated Start	Slave Address + R	A	RAM Data	NA	Stop

Command #10 - Read SFR

Start	Slave Address	A	0x10	A	ADDR LSB	A	ADDR MSB	A	Repeated Start	Slave Address + R	A	SFR Data	NA	Stop

Note: HPS3KW commands are written in blue text.

LEGEND:

(white box)	- From Master
(grey box)	- From Slave

1.7 Set Control Register Command (Command #1)

Set Control Register Command will write the Writable bits of the Control Register of the power supply. The format of this command will be as follows:

MCU Command Syntax and Packet Length:

Command 1: Set Control Register
Writes: 4 bytes
Syntax: CMD#1, new cont reg, new cont reg, LSB of previous 2 bytes
Reads: none

Power Supply Address or General Call
Set Control Register Command (Command #1)
Control Register Value
Control Register Value
LSByte of the sum of previous two bytes

1.8 Read Status Register Command (Command #2)

Read Status Register Command will return the power supply status. The format of this command will be as follows:

MCU Command Syntax and Packet Length:

Command 2: Read Control Status Register
Writes: 1 byte
Syntax: CMD#2
Reads: 1 byte
1. Control Status register

Power Supply Address
Read Status Register Command (Command #2)
Power Supply Address+1
Read Status Byte (Nack)

Reading data from the power supply will be the same as reading from the EEPROM. The exception being that the read command takes the place of the read offset value in the command transaction.

1.9 Read Analog Sensor Data Command (Command #3)

Read Analog Sensor Data Command will return the power supply analog data. The Power supply will respond to the following two formats of this command:

MCU Command Syntax and Packet Length:

Command 3: Read Analog Sensor
Writes: 1 byte
Syntax: CMD#3
Reads: 18 bytes, format 0 of system test mode.(default format)

1. Actual output current lsb
2. Actual output current
3. Actual output current msb
4. Maximum output current lsb
5. Maximum output current
6. Maximum output current msb
7. Minimum usable current lsb
8. Minimum usable current
9. Minimum usable current msb
10. Line voltage lsb centiV
11. Line voltage msb centiV
12. Temperature 1
13. Temperature 1 Fan trip
14. Temperature 1 Supply Fail
15. Temperature 2
16. Temperature 2 Fan Trip
17. Temperature 2 Supply Fail
18. Temperature Update Status 1-new data 0-old data

Note: During AC under-voltage, byte 1 to 11 will not be displayed.

Reads: 4 bytes, format 1 of system test mode

1. Raw ADC Ch0
2. Raw ADC Ch1
3. Raw ADC Ch2
4. Raw ADC Ch3

Reads: 18 bytes, format 2 of system test mode
All bytes should contain 0.

Reads: 18 bytes, format 3 of system test mode
All bytes should contain 1.

Reads: 18 bytes, format 4 of system test mode
Byte read should be alternating 0 and 1.

Single-byte Read Format

Power Supply Address
Read Analog Sensor Data Command (Command #3)
Power Supply Address+1
Read First Byte (Nack)
Power Supply Address+1
Read Second Byte (Nack)
. . .
. . .
Read Byte N (Nack)
Power Supply Address+1
Read Last Byte (Nack)

Multi-byte Read Format

Power Supply Address
Read Analog Sensor Data Command (Command #3)
Power Supply Address+1
Read First Byte (Ack)
Read Byte N (Ack)
Read Last Byte (Nack)

Analog Data Formats

Data read from the power supply will be in the format listed below:

Actual Output Current LSB (milliAmps)	
Actual Output Current (milliAmps)	
Actual Output Current MSB (milliAmps)	
Maximum Output Current LSB (milliAmps)	
Maximum Output Current (milliAmps)	
Maximum Output Current MSB (milliAmps)	
Minimum Usable Output Current LSB (milliAmps)	
Minimum Usable Output Current (milliAmps)	
Minimum Usable Output Current MSB (milliAmps)	
Line Voltage LSB (centi-Volt)	
Line Voltage MSB (centi-Volt)	
*Temperature 1 (^oC)**	
Temperature 1 Fan Trip (^oC)	*35Deg C*
Temperature 1 Supply Fail (^oC)	*40Deg C*
Temperature 2 (^oC)	
Temperature 2 Fan Trip (^oC)	*70Deg C*
Temperature 2 Supply Fail (^oC)	*80Deg C*
*ADC Update Status (1= Updated Data; 0 = Old Data)***	

*In OC condition the Temperature 1 Reading will be obtain by the ADC only when Both the LED's are NOT on simultaneously.
**A value of 1 indicates that the ADC data has been updated since the last I^2C communication to the power supply.

The data read back from the power supply is provided in the smallest unit of available resolution.

- Power supply output current: Output current will be measured as a DC level provided by the power supply interface. This level will then be adjusted using the gain and offset values stored in the EEPROM during calibration. As part of the power supply calibration the lowest usable current reading will be determined and stored in the EEPROM also. Output current shall be reported in milliAmps as a three-byte value.

- Power supply input line voltage: The power supply input line voltage will be measured as a DC level provided by the power supply interface. This level will then be adjusted using the gain and offset values stored in the EEPROM during calibration. Input line voltage will be reported in CENTI VOLTS as a two-byte value.

- Power supply temperature: Two power supply temperature measurements provided as linear DC levels by the power supply interface. The gain and offset values for sensor calibration will be stored in the EEPROM during calibration. Power supply temperatures will be reported in degrees Celsius. In addition to the actual temperature an analog data request will also provide the temperature at which the supply fans will go to full speed and the temperature at which the power supply will cease to operate.

1.10 Test Mode Command (Command #4)

Test Mode will disables the Write Protection to the upper half of the EEPROM allowing the Calibration Test program to write the CAL Table Data into the EEPROM. In this Mode both the Power and the Fail LED will be ON simultaneously. The power supply must be in Standby position for the command to be effective. The power supply will ignore this command if it is turned ON. The format of this command will be as follows:

MCU Command Syntax and Packet Length:

Command 4: Test Mode Command
Writes: 4 bytes
Syntax: CMD#4, CMD#4, CMD#4, sum of preceding 2 bytes
Reads: None
Displays: Both AMBER and GREEN LED ON.

Power Supply Address
Test Mode Command (Command #4)
Test Mode Command (Command #4)
Test Mode Command (Command #4)
LSB of the Sum of Previous two bytes

The only way the power supply can be taken out of the test mode is by recycling the AC power. In test Mode, Temperature 1 Reading will not be available. Command #3 data for Temperature 1 Reading will indicate the Raw ADC reading of the Self-test voltage divider.

1.11 Firmware Debug Command (Command #5)

Firmware debug command returns the Status, Internal Flags and Port Pin Status of the microcontroller. This command will be used to debug the Firmware only. The Firmware Debug Command will respond to the following two formats:

MCU Command Syntax and Packet Length:

Command 5: Firmware Debug Command
Writes: 1 byte
Syntax: CMD#5
Reads: 8 bytes

1. Control Status Register
2. General Flag 1
3. General Flag 2
4. General Flag 3
5. Port 0
6. Port 1
7. Port 2

Single-byte Read Format

Power Supply Address
Firmware Debug Command (Command #5)
Power Supply Address+1
Read First Byte (Nack)
Power Supply Address+1
Read Second Byte (Nack)
. . .
. . .
Read Byte N (Nack)
Power Supply Address+1
Read Last Byte (Nack)

Multi-byte Read Format

Power Supply Address
Firmware Debug Command (Command #5)
Power Supply Address+1
Read First Byte (Ack)
Read Byte N (Ack)
Read Last Byte (Nack)

Firmware Debug Command Data Format

The data format of the Firmware Debug Command Read will be as follows:

Status Register
General Flag 1
General Flag 2
General Flag 3
Port 0
Port 1
Port 2
Port 5

1.12 Firmware Revision Number Command (Command #6)

Firmware Revision Number will be hard coded into the Firmware itself. This command will return the revision number of the Firmware. The Firmware Revision Number Command will respond to the following two formats:

MCU Command Syntax and Packet Length:

Command 6: Firmware Revision Number
Writes: 1 byte
Syntax: CMD#6
Reads: 2 bytes

1. Major Revision Number
2. Minor Revision Number

Single-byte Read Format

Power Supply Address
Firmware Revision Number Command (Command #6)
Power Supply Address+1
Read First Byte (Nack)
Power Supply Address+1
Read Second Byte (Nack)

Multi-byte Read Format

Power Supply Address
Firmware Revision Number Command (Command #6)
Power Supply Address+1
Read First Byte (Ack)
Read Last Byte (Nack)

Firmware Revision Number Data Format

The data format of the Firmware Revision Number Command Read will be as follows:

Major Revision Number
Minor Revision Number

1.13 System Test Mode Command (Command #7)

System Test Mode command will force the power supply to send data in a format specified by the System Test Data Format Command (command #8). This command will toggle the power supply in and out of System Test Mode. This command must be immediately followed by the System Test Data Format Command (Command #8) in order for the power supply to get into the System Test Mode. The format of this Command will be as follows:

MCU Command Syntax and Packet Length:

Command 7:	System Test Mode Command
Writes:	4 bytes
Syntax:	CMD#7, CMD#7, CMD#7, sum of preceding 2 bytes
Reads:	None

Turns ON and OFF system test mode.

Power Supply Address
System Test Mode Command (Command #7)
System Test Mode Command (Command #7)
System Test Mode Command (Command #7)
LSB of the Sum of Previous two bytes

1.14 System Test Data Format Command (Command #8)

System Test Data Format command will specify the format of the data that will be returned by the power supply in response to ADC data request (Command #3) if it is in System Test Mode. This Command is invalid if the power supply is not in System Test Mode and will be ignored by the power supply. The format of this command will be as follows:

MCU Command Syntax and Packet Length:

Command 8: System Test Data Format
Writes: 4 bytes
Syntax: CMD#8, FORMAT#, FORMAT#, sum of preceding 2 bytes
Format # Description

Format #	Description
0	Default, Display processed ADC Data
1	Raw ADC Data
2	All Zero's (0)
3	All One's (1)
4	Alternating Zero's (0) and One's (1)

Reads: none

Sets system test data format for CMD#3.

Power Supply Address
System Test Data Format Command (Command #8)
System Test Data Format
System Test Data Format
LSB of the Sum of Previous two bytes

System Test Data Format

The data format of this command will be as follows:

System Test Data Format	*Format of Data Returned in response to Command #3*
0	*Default Format (Processed ADC data)*
1	*Raw ADC Reading*
2	*All Zero's*
3	*All One's*
4	*Alternate Zero's and One's*
Remaining Values	*Reserved*

1.15 Read RAM Command (Command #9)

The Read RAM Command will return the content of the RAM location specified by Location parameter of this command. Only one RAM location can be read at a time with this command. The Ram Address starts at address 0xFE00. This command will only use the LSB of the address for Location. For example, if RAM location 0xFE20 needs to be read then the value of Location in this command format should be 0x20. The format of this command will be as follows:

MCU Command Syntax and Packet Length:

Command 9: Read RAM Command
Writes: 2 bytes
Syntax: CMD#9, offset address (address starts at 0xFE00)
Reads: 1 byte

Example: 9,62 read data in location 0xFE3E. 3E16 = 6210

Power Supply Address
Read RAM Command (Command #9)
Location
Power Supply Address+1
Read Byte (Nack)

1.16 Read SFR Command (Command #10)

The Read SFR Command will return the content of the SFR specified by Location parameter of this command. Only one SFR can be read at a time with this command. The SFR Address starts at address 0xFF00. This command will use the full address for Location. For example, if the SFR at address 0xFF20 needs to be read then the value of Location LSB should be 0x20 and Location MSB should be 0xFF in this command format. The format of this command will be as follows:

MCU Command Syntax and Packet Length:

Command 10: Read SFR Command
Writes : 3 bytes
Syntax: CMD#10, addr LSB, addr MSB (address starts at 0xFF00)
Reads: 1 byte

Example 10,05,255 read data in address 0xFF05. FF16 = 25510

Power Supply Address
Read RAM Command (Command #10)
Location LSB
Location MSB
Power Supply Address+1
Read Byte (Nack)